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10CS46

Fourth Semester B.E. Degree Examination, June/July 2019
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. Explain the different functional units of a digital computer. **(06 Marks)**

b. List and explain the technological features and devices improvement made during different generations of computers. **(08 Marks)**

c. Perform the following operations on the 5 – bit signed numbers using 2's complement
i) (-11) + (-12) ii) (-11) – (+3). Also indicate whether overflow has occurred. **(06 Marks)**

2 a. With a neat diagram, describe input and output operations. **(08 Marks)**

b. Explain different rotate instructions with examples. **(06 Marks)**

c. What is little endian and big endian memory? Represent the number 6848502CH in 32-bit big – endian and little endian memory. **(06 Marks)**

3 a. With neat sketches, explain various methods for handling multiple interrupt requests. **(12 Marks)**

b. What you mean by direct memory access? With a neat sketch, explain use of DMA controllers in a computer system. **(08 Marks)**

4 a. Explain with a neat block diagram, the hardware components needed for connecting a keyboard to a processor. **(08 Marks)**

b. With a neat figure, explain the tree structure and different packet formats of USB. **(08 Marks)**

c. List the SCSI bus signals with their functionalities. **(04 Marks)**

PART - B

5 a. With a neat sketch, describe the principles of Optical disks. **(06 Marks)**

b. Define Virtual memory techniques. With a diagram, explain how virtual memory address is translated. **(08 Marks)**

c. With a neat figure, explain about direct mapping cache memory. **(06 Marks)**

6 a. Explain Booth algorithm. Apply Booth algorithm to multiply the signed numbers (-13) and (+11). **(10 Marks)**

b. Explain with figure, the design and working of a 16-bit carry – look – ahead adder built from 4 – bit address. **(10 Marks)**

7 a. With a neat block diagram, explain hardwired control unit organisation. Show the generation of Z_{in} and End control signals. **(10 Marks)**

b. Draw and explain three bus organisation of data path. Mention its advantages. **(10 Marks)**

8 a. Define and discuss Amdahl's law. **(06 Marks)**

b. With a diagram, explain a shared memory multiprocessor architecture. **(06 Marks)**

c. What is hardware multithreading? Explain the different approaches to hardware multithreading. **(08 Marks)**

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